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Impact of source-drain series resistance on drain current mismatch in advanced Fully Depleted SOI n-MOSFETs

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***Abstract*— In this study, we show that the source-drain series resistance mismatch exists and that it affects the variability of the drain current in relation to the other mismatch factors. In order to do this, we provide a brand-new approach based on the Y-function for the analysis of drain current mismatch, which enables a precise identification of the numerous sources of variability in cutting-edge FD-SOI MOS devices.**

***Index Terms*— Static mismatch variability, matching, Y-function, characterization, CMOS.**

I. INTRODUCTION

Drain current variability is one of the most critical issues while scaling down the CMOS devices. It has been recognized since the beginning of mismatch studies that the threshold voltage V_{th} and the current gain factor β local fluctuations are the major sources of drain current I_d variability [1,2], both impacting analog and logic circuits like SRAM cells. The advent of ultra-thin body technologies such as Fully Depleted SOI or FinFET has seriously improved the V_{th} variability [3,4], but it has raised new challenges related to the influence of source-drain (SD) series resistance R_{sd} and its variability [5].

In this work, we propose a new methodology for the drain current mismatch study, enabling a precise determination of the various variability sources in advanced FD-SOI MOS devices. In particular, we demonstrate, for the first time, that the source-drain series resistance mismatch is observable in FD-SOI n-MOSFETs, and compare its impact on drain current variability with that of mismatch in other transistor parameters.

II. DEVICES AND MEASUREMENT SETUP

Electrical measurements were performed on n-MOS transistors issued from an advanced FD-SOI CMOS

technology. The gate stack consists of TiN/Hf-based oxide dielectric with equivalent oxide thickness 1.2nm. The minimum channel length (L) is 20nm. Static measurements of the drain current I_d were performed on paired transistors as function of gate voltage V_g, in linear region with Agilent B1500/1530 Semiconductor Device Analyzer. The two MOSFETs of the paired test structure are spaced by the minimum allowed distance, placed in identical environment and electrically independent with symmetric connections. The drain voltage was 50mV and the back gate was grounded. In order to study the static variability of the MOS transistor response, we repeated the drain current measurements of the paired transistors to full wafer.

III. Experimental Results

The drain current mismatch $\Delta I_d/I_d$ for the transistor pair is normally calculated from the linear difference of the two drain current values of the pair $(I_{d2}-I_{d1})/I_{d1}$. However, the use of the standard linear difference of current could lead to not meaningful results when I_{d2}/I_{d1} becomes very small or very large, artificially saturating to one or zero, respectively. For this reason, in this work we propose to evaluate the drain current mismatch from the logarithmic difference of the two drain current values. Therefore, keeping the same notation for simplicity, we define the drain current mismatch as:

$$\frac{\Delta I_d}{I_d} \equiv \ln\left(\frac{I_{d2}}{I_{d1}}\right) \quad (1)$$

Indeed, for small change of the two currents, the logarithmic ratio of Eq. (1) reduces to the usual linear difference since $\ln(I_{d2}/I_{d1}) \approx (I_{d2}-I_{d1})/I_{d1}$, which is conventionally used in matching analysis.

Fig. 1 shows typical $\Delta I_d/I_d(V_g)$ characteristics obtained on a large number of transistor pairs for small (a) and large (b) area devices. As can be seen in Fig. 1(a), $\Delta I_d/I_d$ as defined in (1) can reach values up to 2 below threshold (here $V_{th} \approx 0.3$ V), indicating that the current ratio difference could attain a value almost one decade in weak inversion for small area devices. Interestingly, it should be noted that in large area devices [see Fig. 1(b)], there are cases where $\Delta I_d/I_d$ is larger above threshold, revealing a noticeable difference in $\Delta I_d/I_d(V_g)$ behavior. Note that the strong dispersion of the drain current mismatch at strong inversion has been observed also in other SOI technologies (not presented). This confirms that the behavior of Fig. 1(b) is not specific to a particular lot, but it is characteristic of advanced SOI technologies. As will be shown

later, this feature can be interpreted by SD access resistance R_{sd} effect.

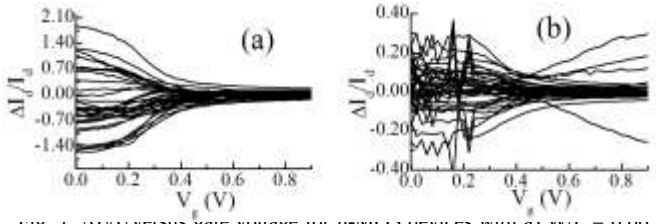

Fig. 1. $\Delta I_d/I_d$ versus gate voltage for n-MOS devices with a) W/L = 0.06 µm / 0.02 µm and b) W/L = 0.3 µm / 0.35 µm.

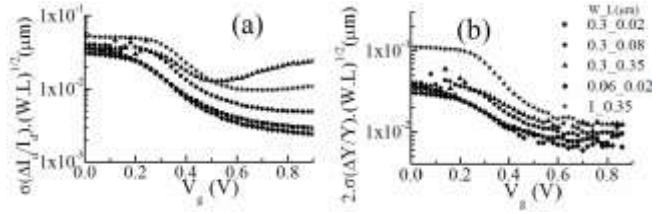

Fig. 2. Standard deviation of (a) $\Delta I_d/I_d$ and (b) of $\Delta Y/Y$ normalized with the square root of device area for n-MOS versus gate voltage.

The standard deviation of the drain current mismatch $\sigma(\Delta I_d/I_d)$ was then calculated for all the dies and plotted as a function of the gate voltage for various device geometries (Fig. 2a). For small area devices, $\sigma(\Delta I_d/I_d)$ vs V_g follows the conventional behavior predicted by Croon's model [2] given by:

$$\sigma\left(\frac{\Delta I_d}{I_d}\right)^2 = \left(\frac{g_m}{I_d}\right)^2 .\sigma(\Delta V_{th})^2 + \sigma(\Delta\beta/\beta)^2 \quad (2)$$

i.e. reaching a maximum plateau in weak inversion, where $\beta=(W/L).C_{ox}\mu_0 V_d$, μ_0 being the low field mobility, C_{ox} the equivalent oxide capacitance per unit area and V_d the drain voltage bias.

In contrast, in large area devices, $\sigma(\Delta I_d/I_d)(V_g)$ characteristics strongly deviate from the standard behavior with a pronounced increase in strong inversion. As already suggested in Fig. 1(b) and anticipated by Rahhal's model [5], this phenomenon could be related to additional R_{sd} mismatch. In fact, in the presence of R_{sd} variability, Croon's model is no longer appropriate and the drain current mismatch reads [5],

$$\sigma\left(\frac{\Delta I_d}{I_d}\right)^2 = \left(\frac{g_m}{I_d}\right)^2 .\sigma(\Delta V_{th})^2 + (1-G_d.R_{sd})^2.\sigma(\Delta\beta/\beta)^2 + \\ + G_d^2.\sigma(\Delta R_{sd})^2 \quad (3)$$

where $\sigma(\Delta R_{sd})^2$ is the variance of the SD series resistance and G_d is the channel conductance ($=I_d/V_d$ in linear region). Eq. (3) clearly reveals that $\sigma(\Delta I_d/I_d)^2$ could increase as G_d^2 in strong inversion if $\sigma(\Delta R_{sd})$ is large enough, in qualitative agreement with the observation of Fig. 2(a). It should also be noted from Eq. (3) that the channel contribution stemming from $\sigma(\Delta V_{th})^2$ and $\sigma(\Delta\beta/\beta)^2$ mainly scales as 1/(WL), whereas the SD access resistance contribution arising from $\sigma(\Delta R_{sd})^2$ mostly varies as G_d^2, i.e. as $(W/L)^2$.

In order to confirm this access resistance mismatch effect, following Rahhal's work [5], for mismatch analysis we propose to use the Y-function $Y(V_g) = I_d/(g_m)^{1/2}$ $[A^{1/2}V^{1/2}]$ [6], since it is immune to SD series resistance effect [7]. The Y parameter mismatch of the paired transistors is calculated following Eq. (1) as $\Delta Y/Y=\ln(Y_2/Y_1)$. After some calculations, it is easy to show that the Y-function mismatch can be equated from weak to strong inversion to:,

$$\sigma\left(\frac{\Delta Y}{Y}\right)^2 = \frac{\beta.\sigma(\Delta V_{th})^2}{4.\beta.n^2.(kT/q)^2 + Y^2} + \frac{1}{4}\sigma\left(\Delta\beta/\beta\right)^2 \quad (4)$$

where n is the subthreshold slope ideality factor ($n \approx 1$ in FD-SOI devices) and kT/q is the thermal voltage.

In strong inversion, $Y \approx \sqrt{\beta}.(V_g-V_{th})$ [6], yielding for the Y-function mismatch:,

$$\sigma\left(\frac{\Delta Y}{Y}\right)^2 \approx \frac{\beta.\sigma(\Delta V_{th})^2}{Y^2} + \frac{1}{4}\sigma\left(\Delta\beta/\beta\right)^2 \quad (5)$$

Eq. (5) clearly indicates that, contrarily to Eq. (3), the Y-function mismatch is not affected by R_{sd} mismatch in strong inversion.

Fig. 2(b) shows the Y-function mismatch, $\sigma(\Delta Y/Y)$, variations with V_g associated to the drain current mismatch of Fig. 2(a). As can be seen, below threshold $2.\sigma(\Delta Y/Y)$ attains a plateau similar to $\sigma(\Delta I_d/I_d)$, as predicted by Eq. (4). In strong inversion, $\sigma(\Delta Y/Y)$ does not exhibits any increase with V_g in agreement with Eq. (5), unlike that of $\sigma(\Delta I_d/I_d)$ shown in Fig. 2(a) for large devices. This confirms that the mismatch obtained by the Y-function does not change with the R_{sd} variability and, hence, that the drain current mismatch rise seen in strong inversion in Fig. 2(a) does stem from the R_{sd} variability. According to Eq. (5), the plot of $Y^2.\sigma(\Delta Y/Y)^2$ versus Y^2 should be a straight line with slope providing the current gain factor mismatch, $\sigma(\Delta\beta/\beta)$, free from the R_{sd} effect as shown in Fig. 3.

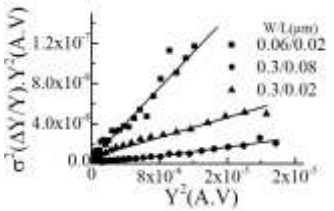

Fig. 3. Linear plot of $Y^2.\sigma(\Delta Y/Y)^2$ against Y^2 used for the extraction of $\sigma(\Delta\beta/\beta)$ based on Eq. (5) for various n-MOS transistors.

Once the current gain factor mismatch has been extracted using the Y-function, we employed Eq. (3) to fit $\sigma(\Delta I_d/I_d)$ versus V_g with $\sigma(\Delta R_{sd})$ as an adjustment parameter. This is displayed in Fig. 4(a) for both large and small area devices. For comparison, we have also shown the results obtained by Croon's model of Eq. (2), which is clearly unable to fit the data for large area devices. The $\sigma(\Delta Y/Y)$ vs V_g data were also nicely fitted using Eq. (5) with no need of $\sigma(\Delta R_{sd})$ [Fig. 4(b)]. All these features clearly demonstrate that the drain current mismatch increase observed in strong inversion for large devices originates from the R_{sd} mismatch contribution.

This procedure was applied to the different geometries shown in Fig. 2, allowing to obtain the Pelgrom plot of Fig. 5.

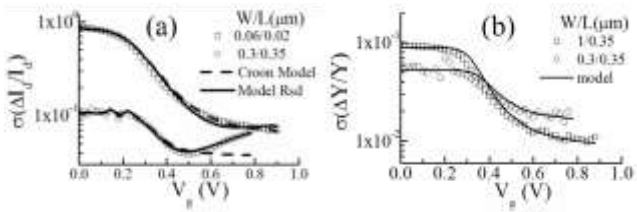

Fig. 4. Comparison between experimental and modeling results for a) $\sigma(\Delta I_d/I_d)$ and b) $\sigma(\Delta Y/Y)$ versus V_g for various geometries.

The V_{th} matching parameter $A_{\Delta Vth}$ exhibits a very low value of 1±0.05 mV.µm, which is at the state-of-the-art for undoped thin film CMOS devices [3,4]. The current gain factor matching parameter $A_{\Delta\beta/\beta}$ takes values around 1±0.1 %.µm, also in line with typical results obtained on advanced CMOS technologies [5,7]. The values extracted for $\sigma(\Delta R_{sd})$ lie around 1200 Ω (resp. 500 Ω) and represent 10% (resp. 20%) of R_{sd} value for W = 0.06 µm (resp. W = 0.3 µm). No specific trend of $\sigma(\Delta R_{sd})/R_{sd}$ with channel W was observed. More statistical studies should be performed in a future work, which is beyond the scope of the present work, dedicated to first demonstration of the impact of R_{sd} mismatch owing to proper methodology of extraction.

In order to underline the role of scaling on R_{sd} mismatch, the typical evolution with device area of the percentage of channel and SD series resistance mismatch contribution to the total drain current variability with device area was evaluated using Eq. (3) for various geometries (Fig. 6). This figure reveals that, in agreement with the scaling feature of Eq. (3) and the trend of the experimental data, the SD series resistance mismatch contribution is enhanced in large (W/L) devices, whereas it could attain 50 to 80 % in short channel devices (L = 0.02 µm). This finding emphasizes the importance of improving the SD access resistance, but also its variability, in advanced CMOS technologies.

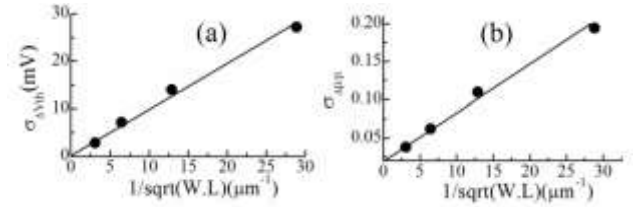

Fig. 5. Pelgrom plot of $\sigma_{\Delta vth}$ (a) and $\sigma_{\Delta\beta/\beta}$ (β) versus the inverse square root of device area, respectively.

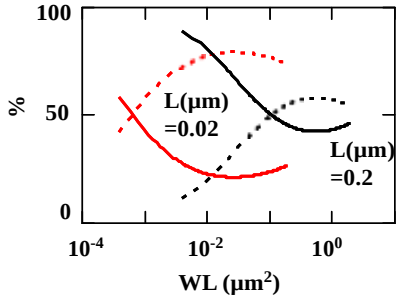

Fig. 6. Percentage contribution of channel (solid line) and SD series resistance (dashed line) mismatch to total drain current variability as obtained from Eq. (3). Parameters: $A_{\Delta Vth}$ = 1mV.µm, $A_{\Delta\beta/\beta}$ = 1%.µm and $\sigma(\Delta R_{sd})$ = 10%.R_{sd} with R_{sd} = 800 Ω.µm)

IV. CONCLUSIONS

A thorough technique for the Y-function-based drain current mismatch investigation has been provided, allowing for a precise identification of the many sources of variability in cutting-edge FD-SOI MOS devices. It has been demonstrated that the SD series resistance mismatch exists and that it has an effect on the variability of the drain current in relation to the other mismatch components. Finally, it was shown that large width and small length devices exhibit a prominent series resistance mismatch effect.

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